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Lab 5 Report

ECE 2031 L07

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图片包含 图表

描述已自动生成

**Figure 1.** A simulation waveform for all possible input and output combinations of the decorative light system.

文本

中度可信度描述已自动生成

**Figure 2.** VHDL code used to implement a decorative light system.

图形用户界面, 应用程序

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**Figure 3.** All the necessary signals and acquisition settings of the Signal Tap Logic Analyzer on Quartus.

图形用户界面, 文本, 应用程序

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**Figure 4.** Signal Tap Acquisition to record all possible input and output combinations of the decorative light system with the sample period 0.05 s.